CTP MODULE SPECIFICATION

ITEM NO.: 411-101.010

All information in this technical data sheet is tentative and subject to change without notice.

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2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	28/NOV/22	All	All	Initial Preliminary	ESR-221026001

Error and omissions excepted – Observe notice of protected rights in accordance to DIN34 / ISO16016

3. GENERAL DESCRIPTION

3.1 OVERVIEW

This is a 10.1" (10.1" diagonal) a-Si & transmissive type thin film transistor liquid crystal display (CTP-LCD) module with LVDS interface. The module is composed of a CTP-LCD panel, driver circuit, and backlight unit.

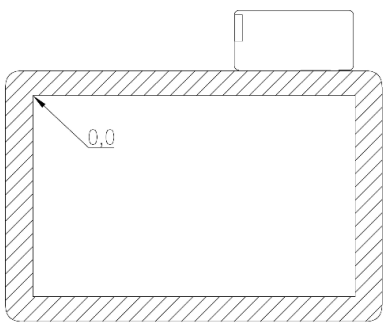
3.2 TFT LCD MODULE SPECIFICATIONS

The following items are characteristics summary on the table under 25°C condition:

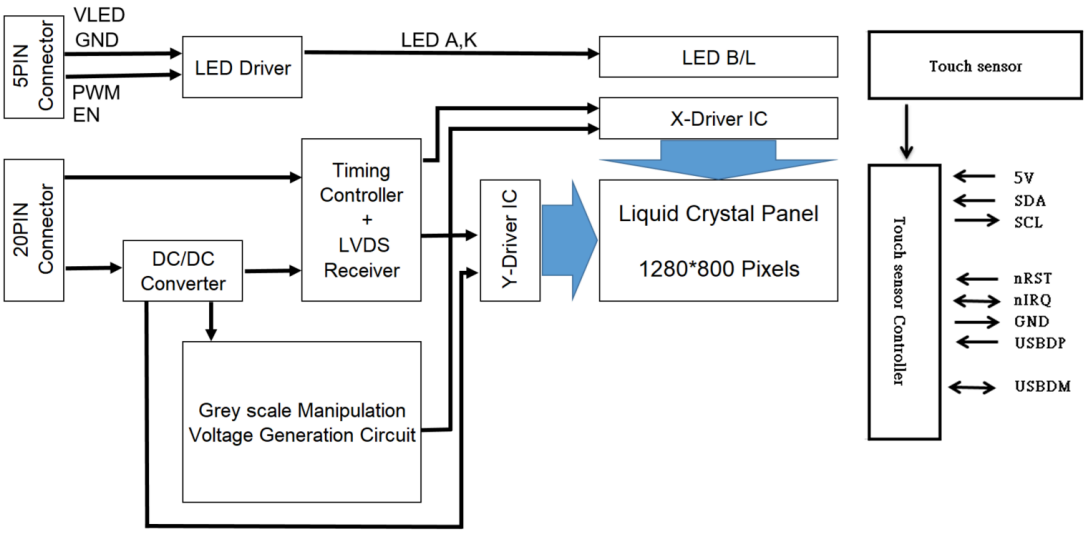
Parameter	Specifications	Unit
Screen Size	10.1(diagonal)	inch
LCD Outline Dimension	252.32(H) x 167.2(V) x 13.8Max.(D)	mm
LCD Active Area	216.96(H) x 135.6(V)	mm
Resolution	1280(H) x (R,G,B) x 800(V)	dots
Pixel Pitch	0.1695(H) x 0.1695(V)	mm
Pixel Arrangement	RGB Vertical stripe	
Display Mode	Normally Black	
View Direction	All	
Luminance, White	850	cd/m^2
LCD Interface	LVDS	
Surface Treatment	Clear	
RoHS Compliance	Yes	

3.3 TFT LCD MODULE SPECIFICATIONS

The following items are characteristics summary on the table under 25°C condition:

Parameter	Specifications	Unit
Touch Type	Transparent type projected capacitive touch panel	
Cover Thickness	1.8	mm
Surface Hardness	7	H
Cover Outline Dimension	252.32(H) x 167.2(V) x 1.8.(D)	mm
Cover Visual Area	216.16(H) × 134.8(V)	mm
Sensor Outline Dimension	233(H) x 155.84(V)	mm
Sensor Active Area	219.76(H) x 138.4(V)	mm
Touch & LCD Bonding	Air Bonding	
Multi-Touch Point	10	
Touch Interface	I^2C USB	
(X, Y) Position		

4. FUNCTIONAL BLOCK DIAGRAM



5. ABSOLUTE MAXIMUM RATINGS

.5.1 ABSOLUTE RATINGS OF ENVIRONMENT

Parameter	Symbol	Min.	Max.	Unit	Remark
Operating temperature	Top	-30	80	°C	
Storage temperature	Tst	-30	80	°C	

.5.2 ELECTRICAL ABSOLUTE RATINGS

Parameter	Symbol	Min.	Max.	Unit	Remark
Power voltage	VDD	-0.3	4	V	Note 2
Logic input signal voltage	VSignal	3.0	3.6	V	
Power voltage for LED	VLED	-0.3	26.5	V	
Supply voltage for CTP	5V	-0.3	6	V	

Note 1: Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.
Note 2: Operating temperature 25°C, humidity 55%RH

6. ELECTRICAL SPECIFICATIONS

6.1 ELECTRICAL CHARACTERISTICS

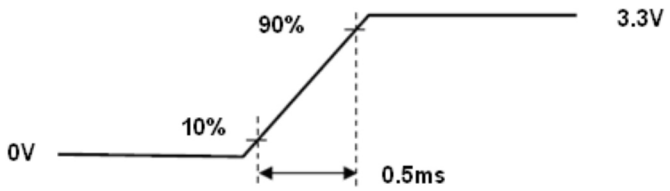
6.1.1 TFT LCD MODULE ELECTRONICS SPECIFICATION

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Power voltage		V_{DD}	3.0	3.3	3.6	V	Note 2, 4
VDD Current	White Pattern	I_{DD}	-	0.27	-	A	Note 3, 4
Rush Current		IRush			1.5	A	Note 1, 4, 5
Allowable Logic/LCD Drive Ripple Voltage		V_{VDD-RP}	-	-	300	mV	Note 4

6.1.2 LED DRIVER UNIT SPECIFICATION

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Power voltage for LED		VLED	10.8	12	13.2	V	
Power current for LED		I_{VLED}	-	620	800	mA	VLED=12V
EN, PWM Signal Logic Voltage	High	VPWM	2	-	VLED	V	
	Low		0	-	0.8	V	
LED_PWM Frequency		FPWM	100	-	1000	Hz	
LED_PWM duty			10-	-	100	%	
LED Life Time			50,000		-	hrs	Note 6

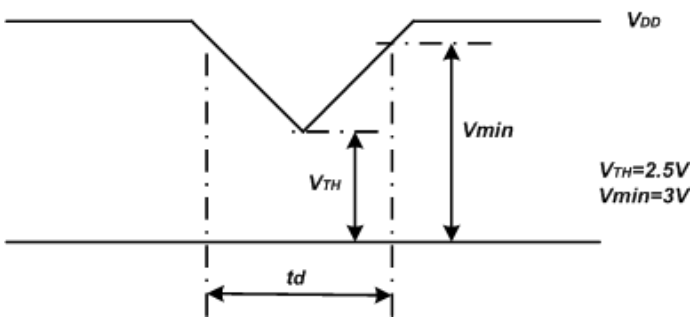
Note 1: Measure Condition



VDD Rising Time

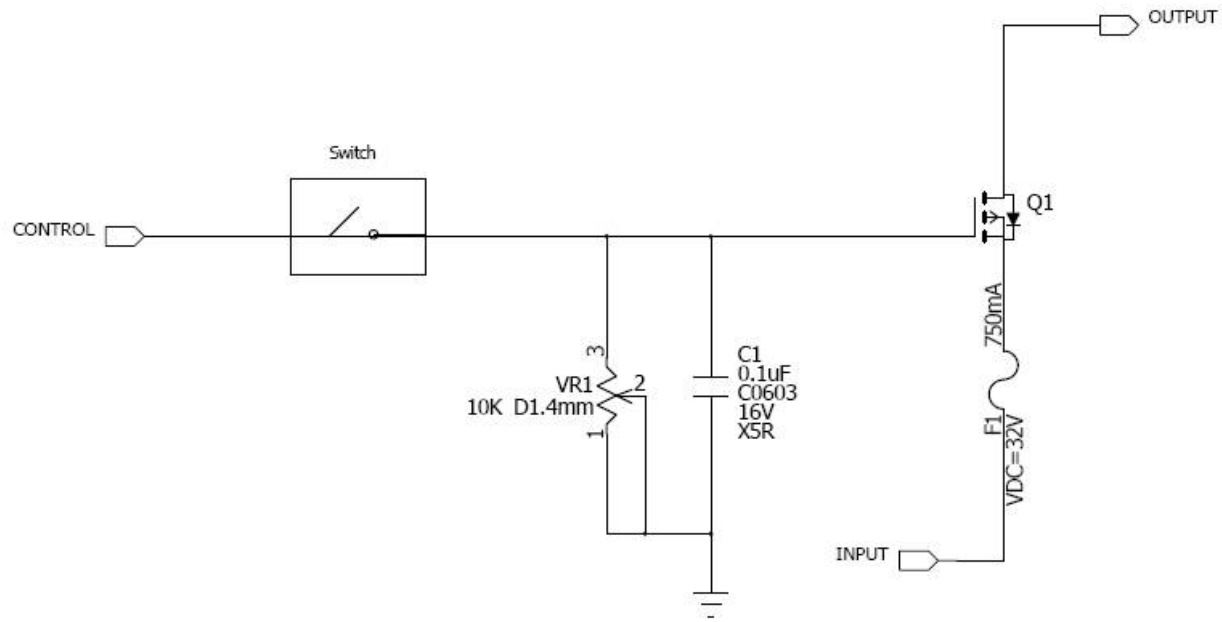
Note 2: VDD Power Dip Condition

VTH < VDD ⩽ Vmin, td ⩽10ms (a time of the voltage return to normal), our panel can revive automatically.



VDD Power Dip

Note 3: Frame Rate=60Hz, VDD=3.3V, DC Current.
Note 4: Operating temperature 25°C, humidity 55%RH.
Note 5:The reference measurement circuit of rush current.



Note 6: The "LED life time" is defined as the module brightness decrease to 50% original brightness at T a=25°C.

6.1.3 TOUCH MODULE ELECTRONIC SPECIFICATION

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
5V	Supply voltage	4.8	5	5.2	V	
I5V	Supply current	-	TBD		mA	5V input
VIH	Input high voltage	2.7	-	-	V	
VIL	Input low voltage	-	-	0.4	V	
VOH	Output high voltage	2.9	-	-	V	I = 2mA
VOL	Output low voltage	-	-	0.4	V	I = 2mA

6.2 SIGNAL CHARACTERISTICS

6.2.1 LVDS RECEIVER

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Differential input high Threshold voltage	RXVTH	-	-	+100	mV	VCM=1.2V
Differential input low Threshold voltage	RXVTL	-100	-	-	mV	
Differential voltage	–VID–	200	-	600	mV	
Common Mode Voltage	V_{CM}	1	1.2	1.4	V	

Note 1: Input signals shall be low or Hi- resistance state when VDD is off.
Note 2: All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

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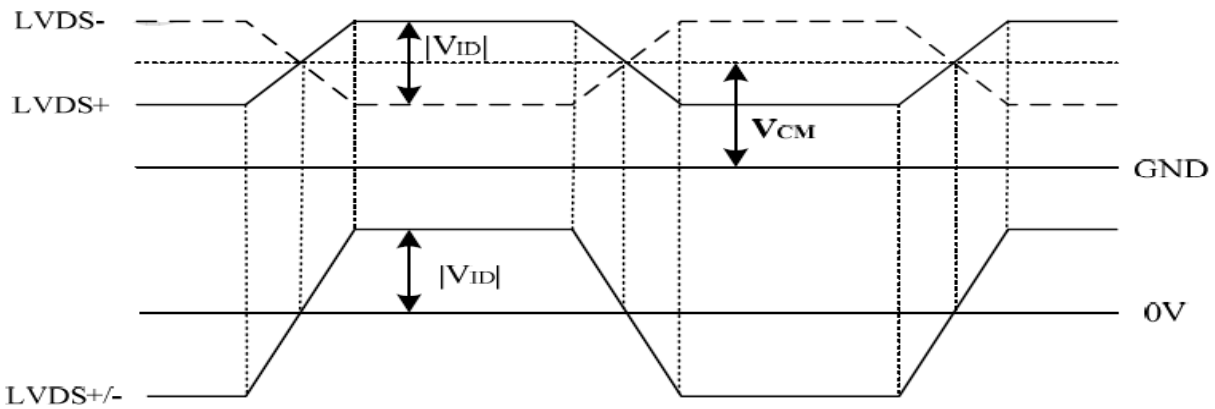
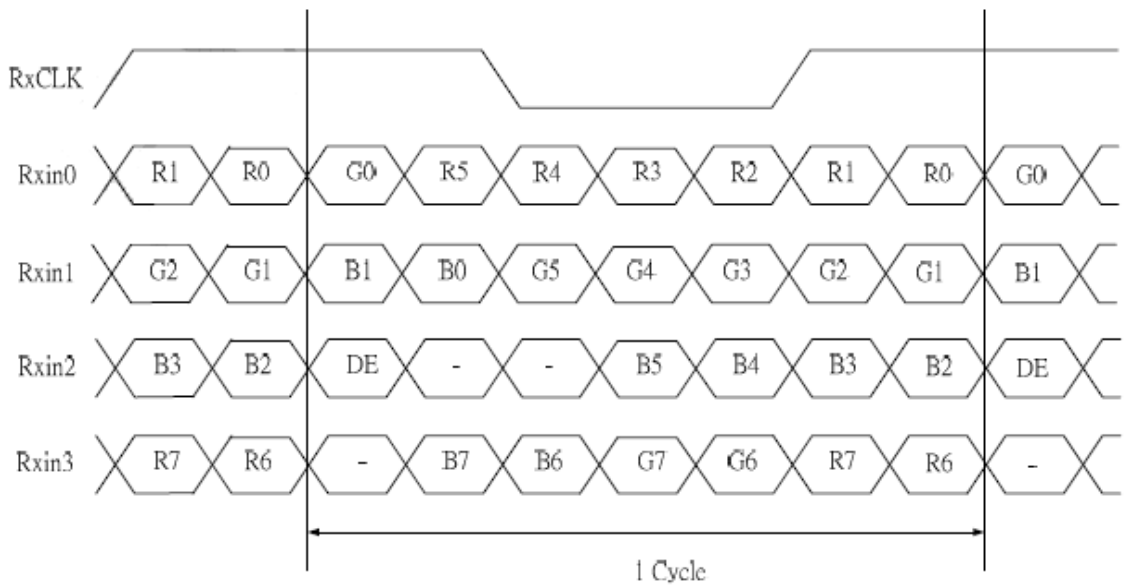
Voltage Definitions

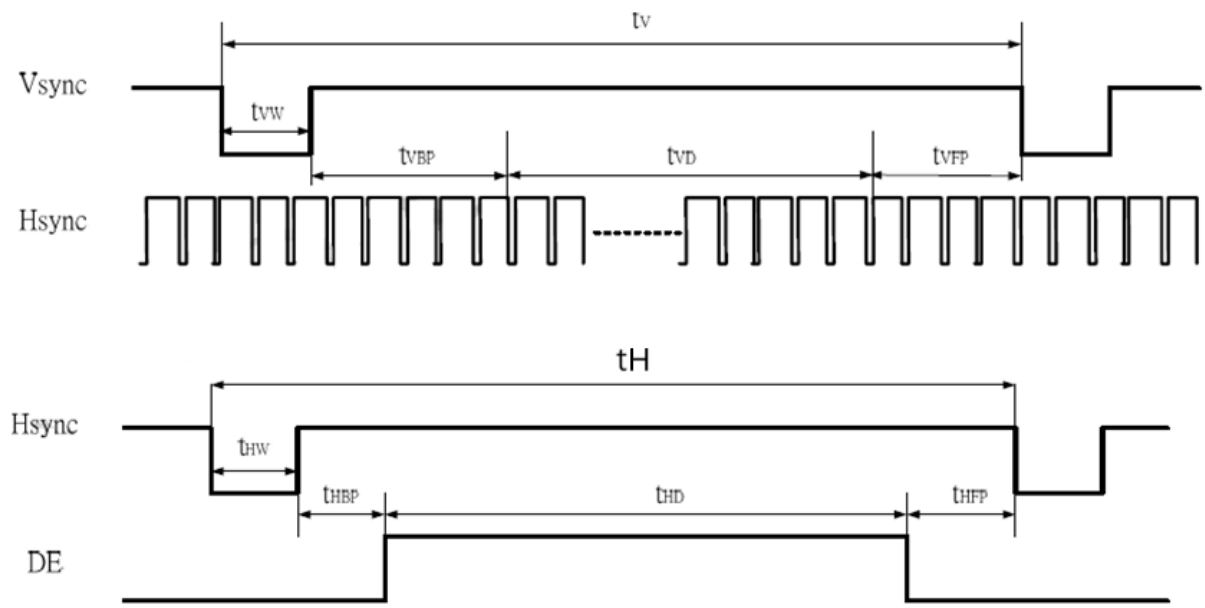


LVDS Data Mapping

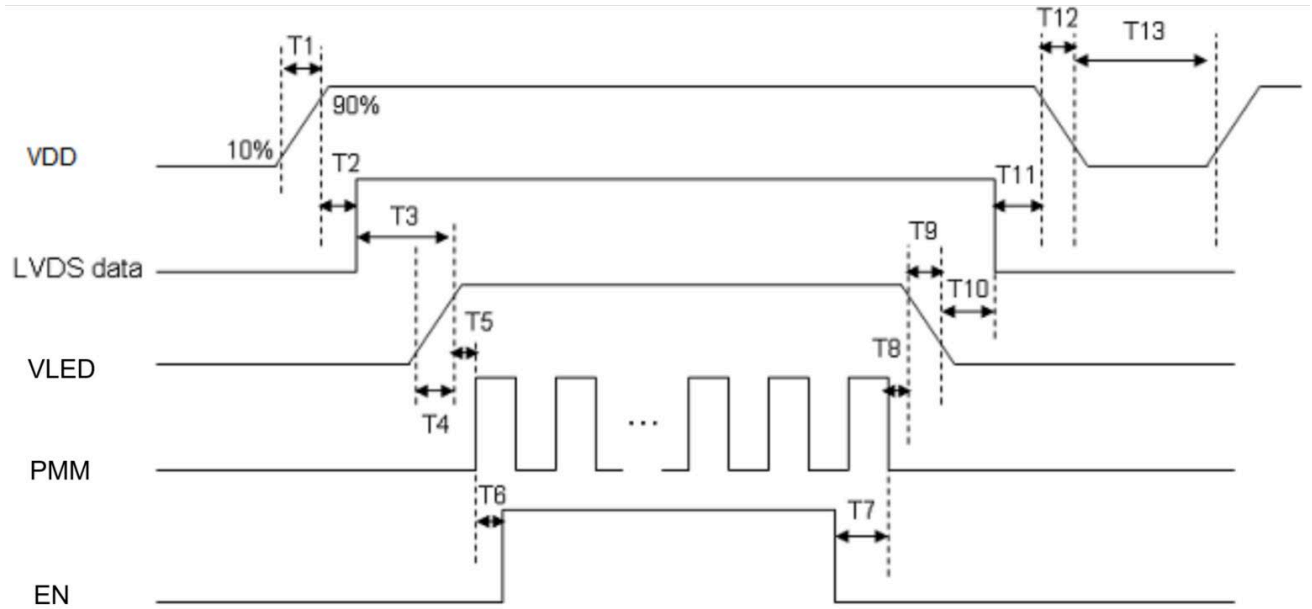


6.2.2 INTERFACE TIMING

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Frame Rate	-	-	60	-	Hz	
Frame Period	tv	824	838	872	line	
Vertical display area	tvd		800		line	
Vertical Blanking Time	tVW+tvBP+tvFP	24	38	72	line	
1 Line Scanning Time	tH	1380	1440	1500	clock	
Horizontal Display Time	tHD		1280		clock	
Horizontal Blanking Time	tHW+tHBP+tHFP	100	160	220	clock	
Clock Rate	1/Tc	66.3	72.4	78.9	MHz	



6.2.3 POWER ON OFF SEQUENCE

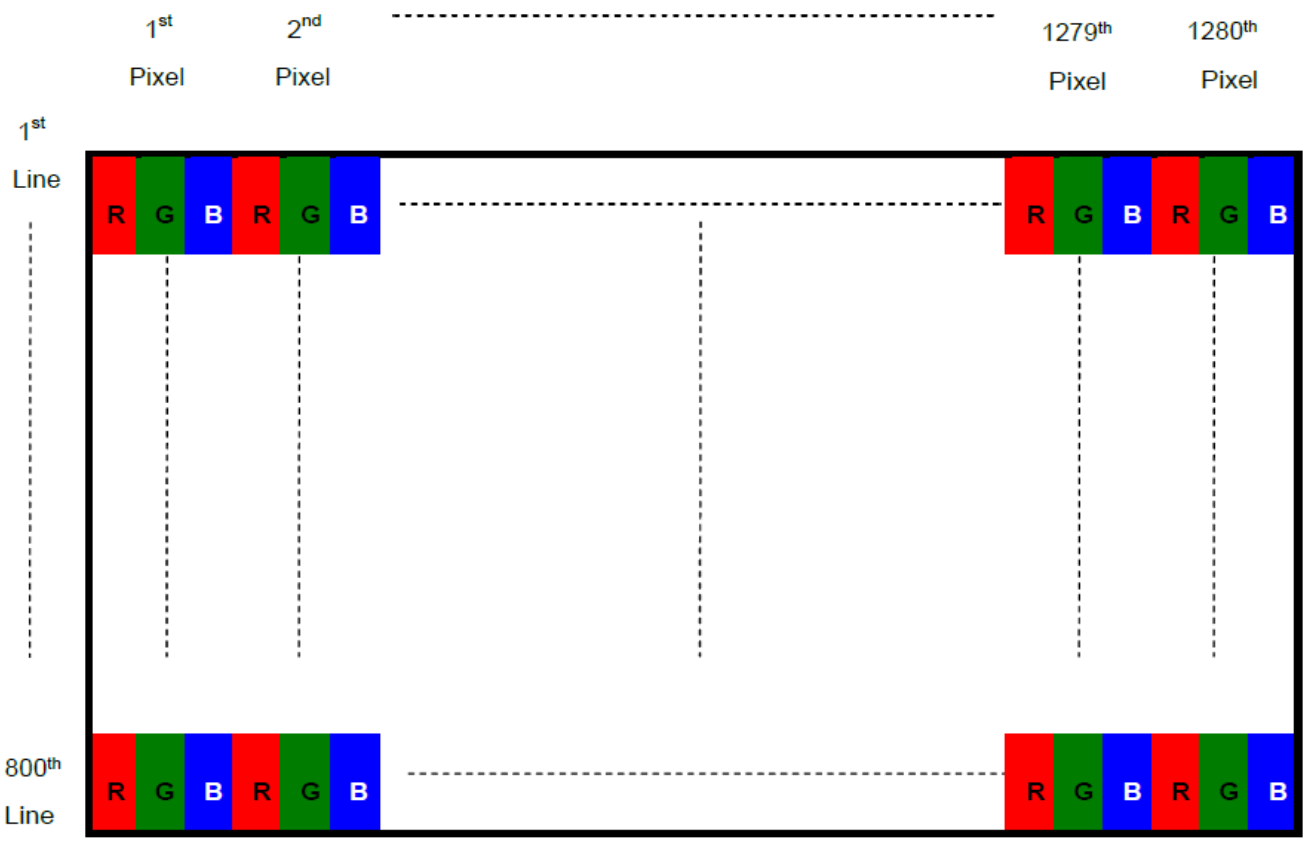


Power Sequencing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
VDD Rise Time	T1	0.5	-	10	ms	
VDD Good to Signal Valid	T2	30	-	90	ms	
Signal Valid to Backlight On	T3	200	-	-	ms	
Backlight Power on Time	T4	0.5	-	-	ms	
Backlight LED_VCCS Good to System PWM on	T5	10	-	-	ms	
System PWM on to backlight enable on	T6	10	-	-	ms	
Backlight enable off to system PWM off	T7	0	-	-	ms	
System PWM off to B/L Power Disable	T8	10	-	-	ms	
Backlight Power off Time	T9	0.5	10	30	ms	
Backlight Off to Signal Disable	T10	200	10	30	ms	
Signal Disable to Power Down	T11	0	-	50	ms	
VDD Fall Time	T12	0.5	10	30	ms	
Power Off	T13	500	-	-	ms	

6.3 PIXEL FORMAT IMAGE

Following figure shows the relationship between input signal and LCD pixel format.



6.4 INTERFACE CONNECTIONS

6.4.1 CN1 PIN ASSIGNMENT

Pin No.	Symbol	Function	Remark
1	VDD	Power Supply Voltage	
2	VDD	Power Supply Voltage	
3	GND	Ground	
4	UD	Vertical inversion U/D = "0", set top to bottom scan direction U/D = "1", set bottom to top scan direction	Default is "0"
5	D0-	-LVDS Differential Data Input	
6	D0+	+LVDS Differential Data Input	
7	GND	Ground	
8	D1-	-LVDS Differential Data Input	
9	D1+	+LVDS Differential Data Input	
10	GND	Ground	
11	D2-	-LVDS Differential Data Input	
12	D2+	+LVDS Differential Data Input	
13	GND	Ground	
14	CLK-	-LVDS Differential Clock Input	
15	CLK+	+LVDS Differential Clock Input	
16	GND	Ground	
17	D3-	-LVDS Differential Data Input	
18	D3+	+LVDS Differential Data Input	
19	LR	Horizontal inversion L/R = "0", set right to left scan direction L/R = "1", set left to right scan direction	Default is "0"
20	GND	Ground	

6.4.2 CN1 PIN ASSIGNMENT

Pin No.	Symbol	Function	Remark
1	NC	No connection	
2	PWM	Dimming control for backlight	
3	EN	Enable control for backlight	
4	GND	Ground	
5	VLED	Power supply for LED driver IC	

6.4.3 CTP PIN FUNCTION

Pin No.	Symbol	Function	Remark
1	5V	Power supply input for CTP	
2	SDA	I^2C Data	
3	SCL	I^2C Clock	
4	nRST	Reset, active low	
5	nIRQ	Interrupt output, active low	
6	GND	Ground	
7	USBDP	USB D+	
8	USBBDM	USB D-	
9	NC	No connection	
10	GND	Ground	

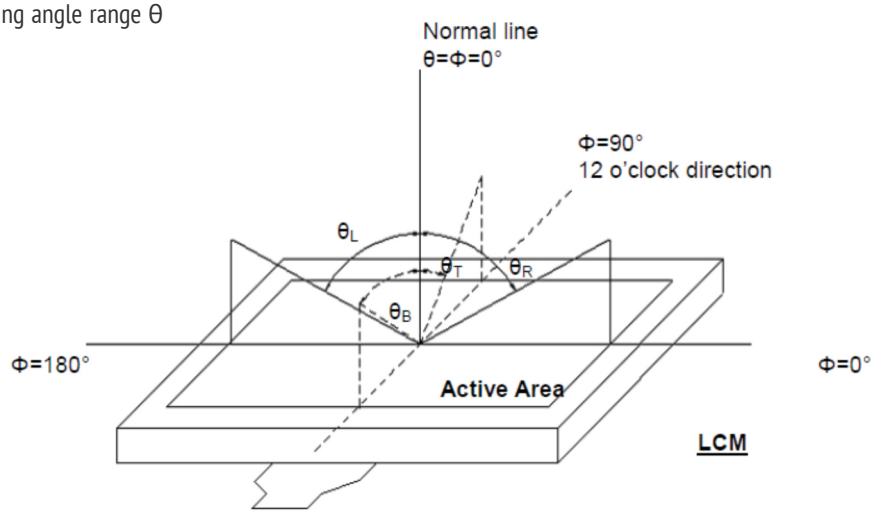
7. OPTICAL SPECIFICATIONS

7.1 Optical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle (CR≥ 10)	θ_L	Φ=180° (9 o'clock)	70	80	-	deg	Note 1
	θ_R	Φ=0° (3 o'clock)	70	80	-		
	θ_T	Φ=90° (12 o'clock)	70	80	-		
	θ_B	Φ=270° (6 o'clock)	70	80	-		
Contrast ratio	CR	Normal θ=Φ=0°	800	1000	-		Note 4
Response time	Rising + Falling		-	25	35	ms	Note 3
Color chromaticity	Wx		Typ. -0.05	0.322	Typ. +0.05	-	Note 5
	Wy			0.344		-	
Luminance	L		760	850	-	cd/m²	Note 6
Luminance uniformity	YU		70	75	-	%	Note 7

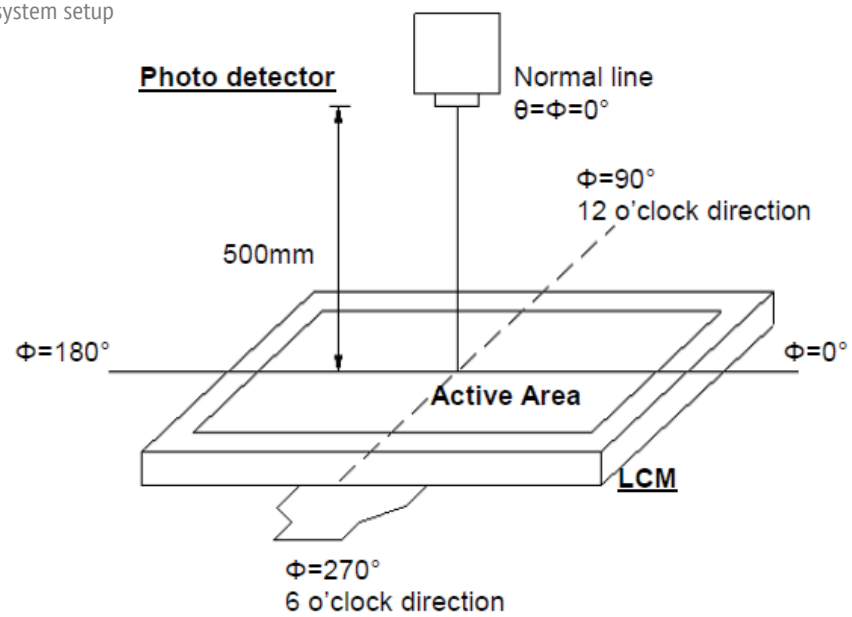
Test Conditions:
1. LED Backlight Current IF=180mA., the ambient temperature is 25°C.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range θ

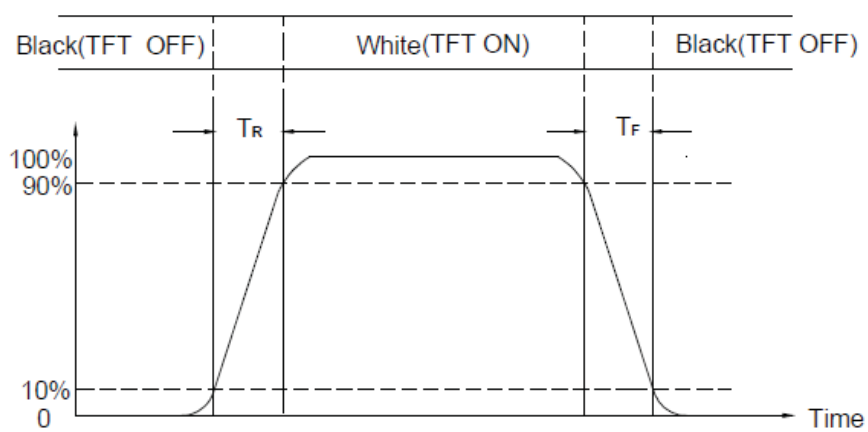


Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 2 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, other items are measured by BM-7A/ Field of view: 1° /Height: 500mm.)

Optical measurement system setup



Note 3: Definition of Response time



Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

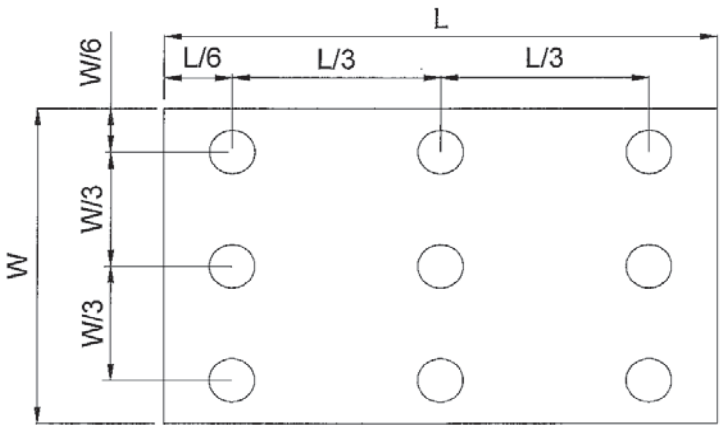
Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: Measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas. Every measuring point is placed at the center of each measuring area.

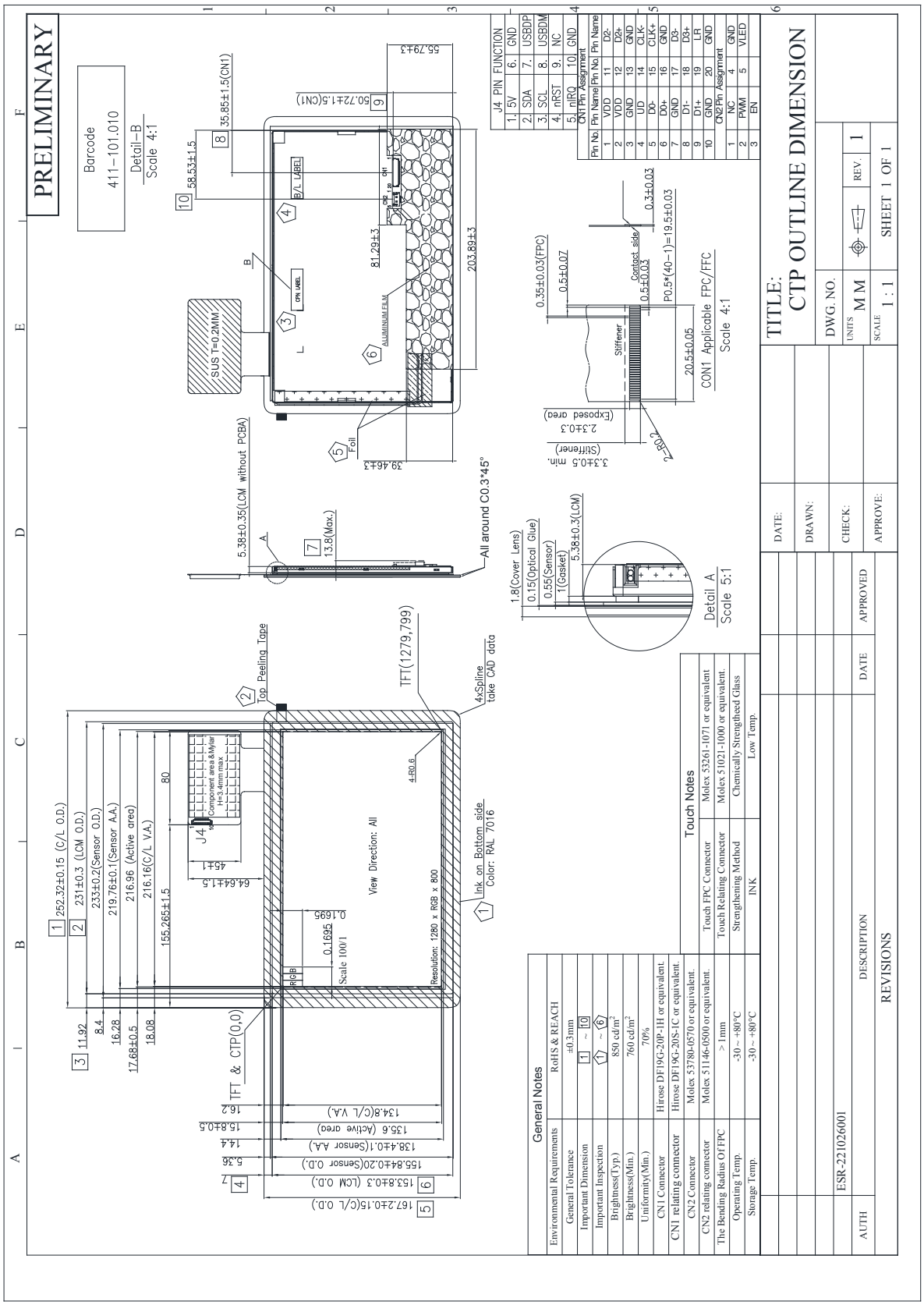
$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L--------Active area length W------ Active area width



8. MECHANICAL SPECIFICATIONS

8.1 OUTLINE DRAWING



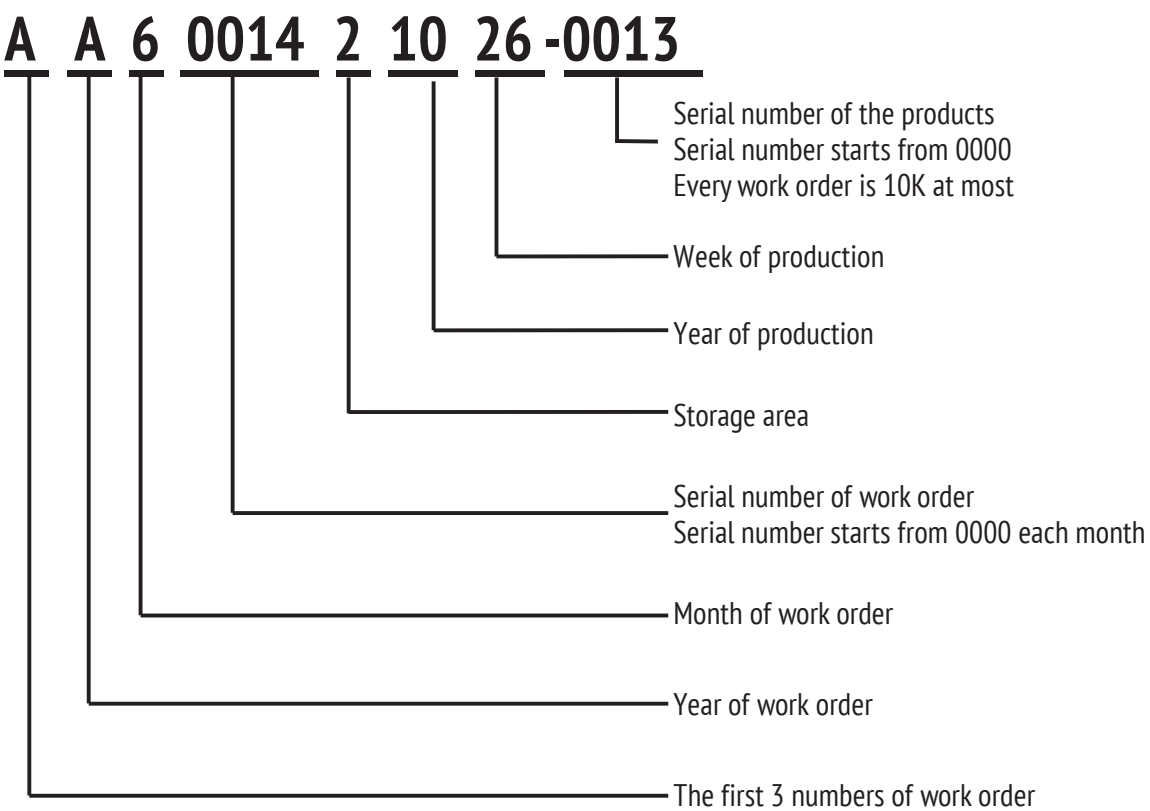
9. RELIABILITY TEST ITEM

No.	Item	Test Conditions	Remark
1	High Temperature Storage Test	Ta=80°C, 240hrs	IEC60068-2-2
2	Low Temperature Storage Test	Ta=-30°C, 240hrs	IEC60068-2-1
3	High Temperature Operation Test	Ts=80°C, 240hrs	IEC60068-2-2
4	Low Temperature Operation Test	Ta=-30°C, 240hrs	IEC60068-2-1
5	High Temperature and High Humidity (No operation)	T=60°C, 90%RH, 240hrs	IEC60068-2-3
6	Thermal cycling storage test (No operation)	-30°C ----25°C ---80°C, 200 Cycle 30min 5min 30min	IEC60068-2-14
7	Vibration test (Package)	Frequency: 10~55HZ Amplitude: 1.5mm Sweep time: 11min Test period: 6 Cycles for each direction of X, Y, Z	IEC60068-2-6
8	Drop test (Package)	Height: 60cm 1 conner, 3 edges, 6 surfaces	IEC60068-2-32
9	Electrostatic Discharge Test	State: operating Location: LCM/TP surface Condition: 150pf 330Ω Contact +/- 4kV Air +/-8kV Criteria: Class C	IEC61000-4-2

10. PRODUCT LABEL DEFINE

Product Label style:

Bar Code Define:



11. PRECAUTIONS IN USE LCM

11.1 HANDLING PRECAUTIONS

a. The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
b. While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
c. Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
d. Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
e. If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
f. Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
g. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
h. Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
i. Do not disassemble the module.
j. Do not pull or fold the LED wire.
k. Pins of I/F connector should not be touched directly with bare hands.

11.2 STORAGE PRECAUTIONS

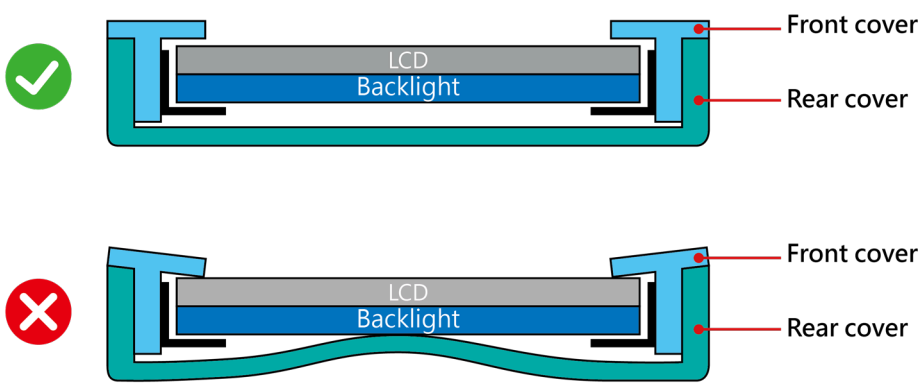
a. High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
b. It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
c. It may reduce the display quality if the ambient temperature is lower than 10 oC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

11.3 OPERATION PRECAUTIONS

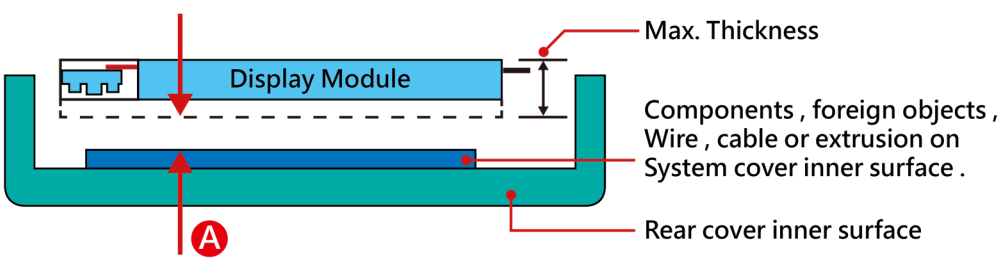
a. Do not pull the I/F connector in or out while the module is operating.
b. Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
c. The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

APPENDIX. COVERS DESIGN GUIDELINE

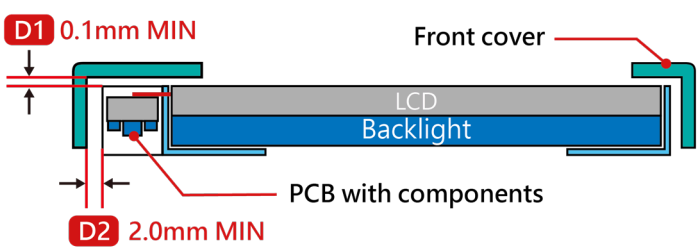
A	**Permanent deformation of front/rear covers after reliability test**



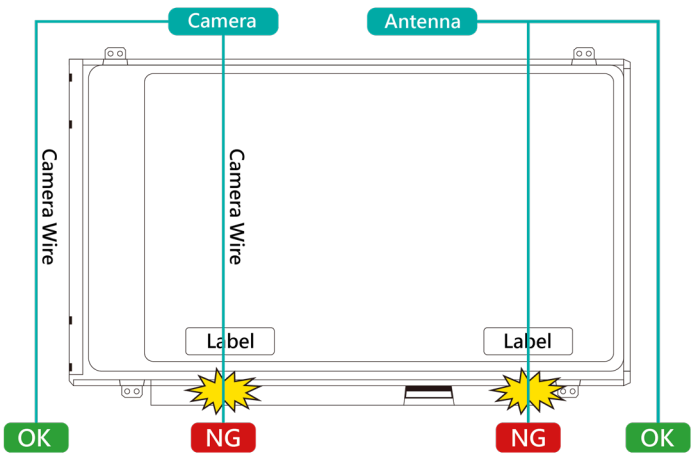
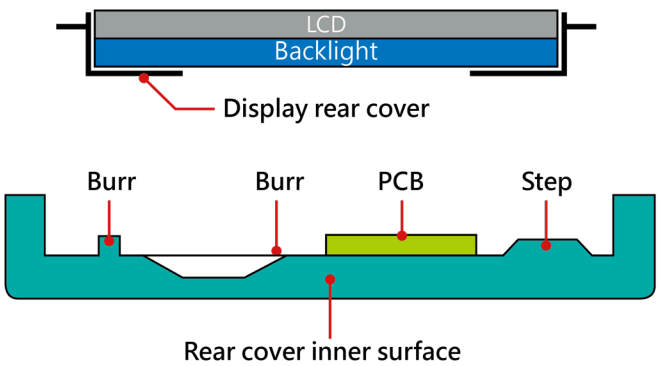
Definition	Front/rear covers may deform during reliability test. Permanent deformation of front/rear covers after reliability test should not interfere with display. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
B	**Design gap A between display and any components on rear cover**



Definition	Gap A between display's maximum thickness boundary and rear cover inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, white spot and cell crack may occur. Flatness of display and rear cover should be taken into account for gap design.
C	**Design gap D1 & D2 between front cover and PCB assembly**

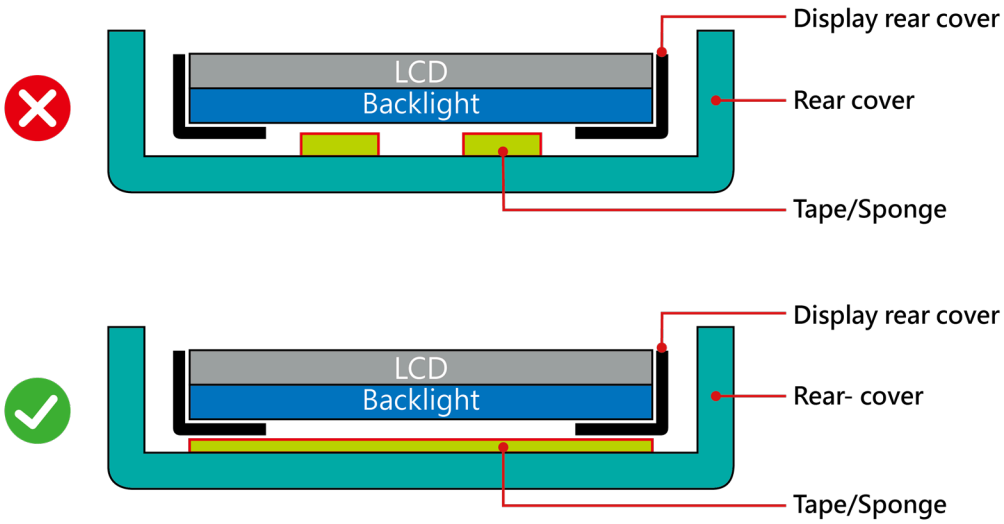


APPENDIX. COVERS DESIGN GUIDELINE

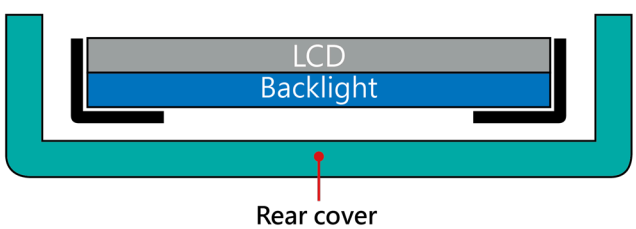
Definition	Gap D1 & D2 between front cover and LCD & front cover and PCBA are needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near front cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum display thickness is recommended.
D	**Interference examination of camera's and antenna's cable**
	
Definition	Camera's and antenna's cable should not overlap with panel outline. Because issue such as abnormal display and white spot after backpack test, hinge test, twist test or pogo test may occur.
E	**Rear cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB may cause stress concentration. Whiter spot or glass broken issue may occur during reliability test.
F	**Tape/sponge design on rear cover inner surface**

Error and omissions excepted – Observe notice of protected rights in accordance to DIN34 / ISO16016

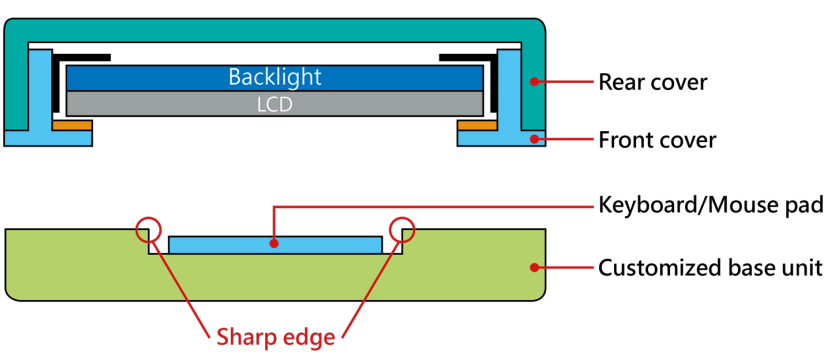
APPENDIX. COVERS DESIGN GUIDELINE



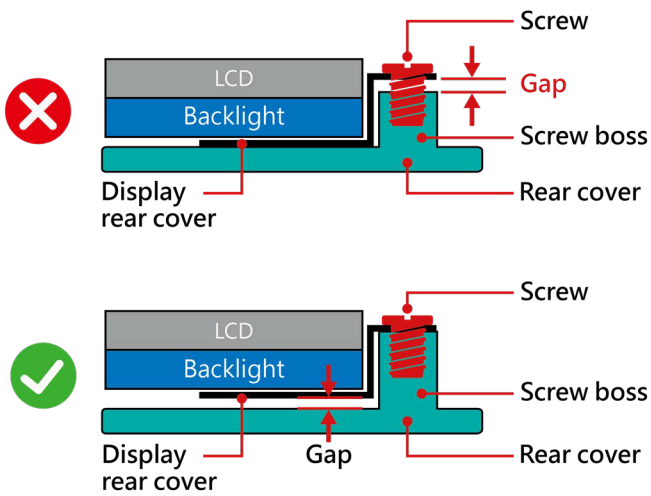
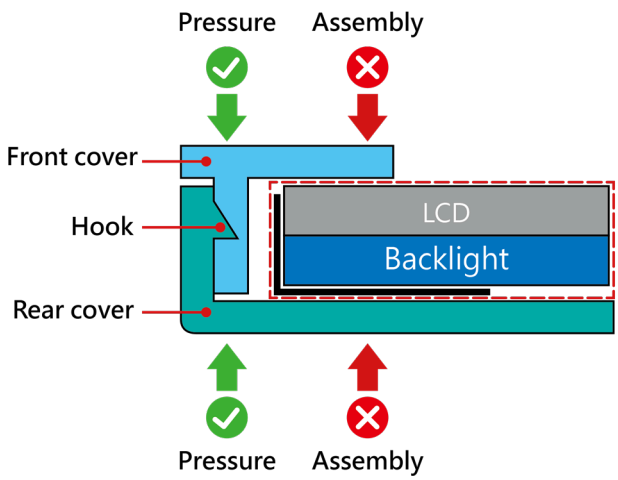
Definition	To prevent abnormal display and white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under rear cover. Because tape/sponge in separate location may act as pressure concentration location.
G	**Material used for rear cover**



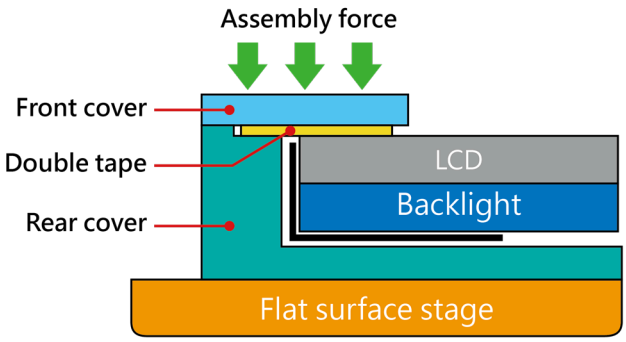
Definition	Rear cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear cover may also influence the rigidity of rear cover. The deformation of rear cover should not caused interference.
H	**Customized base unit design near keyboard and mouse pad**



APPENDIX. COVERS DESIGN GUIDELINE

Definition	To prevent abnormal display and white spot after Scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage display during the test. We suggest to use slope edge design or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
I	**Screw boss height design**
	
Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to display bottom surface with flatness change of display it set. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
J	**Assembly SOP examination for front cover with Hook design**
	
Definition	To prevent display crack during front cover assembly process with hook design, it is not recommended to press display or any location that related directly to the display.

APPENDIX. COVERS DESIGN GUIDELINE

L	Assembly SOP examination for front cover with Double tape design
	
Definition	To prevent display crack during system front cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.